Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	(repair same simulation) and (vhdl or verilog)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 21:12
L2	6	("4717644" | "4758094" | "5598341" | "5686206" | "5994030" | "6483937").PN. OR ("6778695").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 21:18
L3	21	(fuse adj3 list)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 21:19
L4	6	3 and simulat$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 21:19

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	vampire and opus and fuse	USPAT	OR	OFF	2005/06/15 20:31
L2	0	vampire and opus and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:31
L3	0	vampire and opus	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:31
L4	309	vampire	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:31
L5	0	4 and vhdl	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:32
L6	0	4 and verilog	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:32
L7	1	dracula and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:32
L8	45	("4618938" | "4706019" | "4721909" | "4837447" | "4895780" | "5065092" | "5198986" | "5251140").PN. OR ("5392222").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:34
L9	0	8 and fuse	USPAT	OR	OFF	2005/06/15 20:34
L10	4	8 and repair	USPAT	OR	OFF	2005/06/15 20:35
L11	1	verilog adj path	USPAT	OR	OFF	2005/06/15 20:36
L12	64	verilog same path	USPAT	OR	OFF	2005/06/15 20:36
L13	3	12 and fuse	USPAT	OR	OFF	2005/06/15 20:36

L14	7	("5970254" | "6006321" | "6028445" | "6150836" | "6182268" | "6311200").PN. OR ("6539477").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:39
L15	30	repair and (integrated adj circuit) and verilog	USPAT	OR	OFF	2005/06/15 20:39
L16	22	("4722084" | "4876685" | "5255227" | "5270974" | "5598373" | "5764577" | "5764878" | "5970000" | "6006311" | "6065134" | "6081910").PN. OR ("6181614"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:52
L17	2	(verif$7 adj3 repair) and simulation and (vhdl or verilog)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:53
L18	15	("5381417" | "5383167" | "5557531" | "5634115" | "5648909" | "5650938" | "5805861" | "5850348" | "5995955" | "6026220" | "6026228").PN. OR ("6591402"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:54

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	verilog adj2 simulat$5 adj2 netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 19:57
L2	1	verilog same (simulated adj2 netlist)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 19:57
L3	1	(vhdl or verilog) same (simulated adj2 netlist)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 19:57
L4	3	("5732247" | "6167363" | "6208954").PN. OR ("6856950"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 19:58
L5	39	repair and fuse and simulation and (path adj2 data) and repair and verify	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:01
L6	1	("5764878").PN.	USPAT	OR	OFF	2005/06/15 20:03
L7	0	("mapsamefuse").PN.	USPAT	OR	OFF	2005/06/15 20:03
L8	157	map same fuse	USPAT	OR	OFF	2005/06/15 20:03
L9	1	8 and verilog	USPAT	OR	OFF	2005/06/15 20:04
L10	53	8 and (verify or verification)	USPAT	OR	OFF	2005/06/15 20:04
L11	29	10 and repair	USPAT	OR	OFF	2005/06/15 20:04
L12	16	("4051354" | "4648075" | "5058070" | "5379258" | "5644699" | "5764878" | "5781717" | "6141768").PN. OR ("6408401").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:10
L13	24	verilog adj netlist	USPAT	OR	OFF	2005/06/15 20:10
L14	0	13 and enumeration	USPAT	OR	OFF	2005/06/15 20:10
L15	1	13 and enum$8	USPAT	OR	OFF	2005/06/15 20:11
L16	1	13 and repair	USPAT	OR	OFF	2005/06/15 20:11
L17	0	13 and fuse$5	USPAT	OR	OFF	2005/06/15 20:11
L18	17	13 and simulation	USPAT	OR	OFF	2005/06/15 20:14
L19	569	(703/14).CCLS.	USPAT	OR	OFF	2005/06/15 20:14

L20	0	19 and fuse and repair	USPAT	OR	OFF	2005/06/15 20:14

Results for "((fuse <and> repair <and> verilog <and> programmed <and> simulation)<in&g..."

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

No results were found.

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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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((fuse <and> hdl)<in>metadata)

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Display Format: Citation Citation & Abstract

1. **Automatic formal verification of fused-multiply-add FPUs**
Jacobi, C.; Weber, K.; Paruthi, V.; Baumgartner, J.;
Design, Automation and Test in Europe, 2005. Proceedings
2005 Page(s):1298 - 1303 Vol. 2
AbstractPlus | Full Text: PDF(248 KB) IEEE CNF

Results for "((fuse <and> verilog)<in>metadata)"
Your search matched **2** of **1171917** documents.
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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

1. **Architectural design of a fast floating-point multiplication-add fused unit using signed-digit addition**
Chen, C.; Chen, L.-A.; Cheng, J.-R.;
Computers and Digital Techniques, IEE Proceedings-
Volume 149, Issue 4, July 2002 Page(s):113 - 120
AbstractPlus | Full Text: PDF(595 KB) IEE JNL

2. **Architectural design of a fast floating-point multiplication-add fused unit using signed-digit addition**
Chichyang Chen; Liang-An Chen; Jih-Ren Cheng;
Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on
4-6 Sept. 2001 Page(s):346 - 353
AbstractPlus | Full Text: PDF(408 KB) IEEE CNF

Results for "((repair <and> simulation <and> vhdl)<in>metadata)"

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

View: **1-25** | 26-50 | 51-58

1. **Predicting the Location and Number of Faults in Large Software Systems**
Ostrand, T.J.; Weyuker, E.J.; Bell, R.M.;
Software Engineering, IEEE Transactions on
Volume 31, Issue 4, April 2005 Page(s):340 - 355
AbstractPlus | Full Text: PDF(1304 KB) IEEE JNL

2. **From conventional control to autonomous intelligent methods**
RayChaudhuri, T.; Hamey, L.G.C.; Bell, R.D.;
Control Systems Magazine, IEEE
Volume 16, Issue 5, Oct. 1996 Page(s):78 - 84
AbstractPlus | Full Text: PDF(1328 KB) IEEE JNL

3. **Tools that bind: creating integrated environments**
Sharon, D.; Bell, R.;
Software, IEEE
Volume 12, Issue 2, March 1995 Page(s):76 - 85
AbstractPlus | Full Text: PDF(940 KB) IEEE JNL

4. **Tools to engineer new technologies into applications**
Bell, R.; Sharon, D.;
Software, IEEE
Volume 12, Issue 2, March 1995 Page(s):11 - 16
AbstractPlus | Full Text: PDF(924 KB) IEEE JNL

5. **Experimental 6-GHz frozen wave generator with fiber-optic feed**
Thaxter, J.B.; Bell, R.E.;
Microwave Theory and Techniques, IEEE Transactions on
Volume 43, Issue 8, Aug. 1995 Page(s):1798 - 1804
AbstractPlus | Full Text: PDF(644 KB) IEEE JNL

6. **High-voltage onsite commissioning tests for gas-insulated substations using UHF partial discharge detection**
Bell, R.; Charlson, C.; Halliday, S.P.; Irwin, T.; Lopez-Roldan, J.; Nixon, J.;
Power Delivery, IEEE Transactions on
Volume 18, Issue 4, Oct. 2003 Page(s):1187 - 1191
AbstractPlus | References | Full Text: PDF(229 KB) IEEE JNL

7. **Results of NSTX heating experiments**
Mueller, D.; Ono, M.; Bell, M.G.; Bell, R.E.; Bitter, M.; Bourdelle, C.; Darrow, D.S.; Efthimion, P.C.; Fredrickson, E.D.; Gates, D.A.; Goldston, R.J.; Grisham, L.R.; Hawryluk, R.J.; Hill, K.W.; Hosea, J.C.; Jardin, S.C.; Ji, H.; Kaye, S.M.; Kaita, R.; Kugel, H.W.; Johnson, D.W.; LeBlanc, B.P.; Majeski, R.; Mazzucato, E.; Medley, S.S.; Menard, J.E.; Park, H.K.; Paul, S.F.; Phillips, C.K.; Redi, M.H.; Rosenberg, A.L.; Skinner, C.H.; Soukhanovskii, V.A.; Stratton, B.; Synakowski, E.J.; Taylor, G.; Wilson, J.R.;

Results for "(fuse<in>metadata) <and> (verilog<in>metadata) <and> (repair<in>..."

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IEEE STD	IEEE Standard

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(fuse<in>metadata) <and> (repair<in>metadata)

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1-25 | 26-40

1. **On-chip repair and an ATE independent fusing methodology**
Cowan, B.; Farnsworth, O.; Jakobsen, P.; Oakland, S.; Ouellette, M.R.; Wheater, D.L.;
Test Conference, 2002. Proceedings. International
7-10 Oct. 2002 Page(s):178 - 186
AbstractPlus | Full Text: PDF(551 KB) IEEE CNF

2. **Ultraviolet laser repair of advanced semiconductor memory devices**
Baird, B.W.; Nilsen, B.E.; Hainsey, R.F.; Ho Wai Lo;
Lasers and Electro-Optics, 2001. CLEO '01. Technical Digest. Summaries of papers presented at the Conference on
6-11 May 2001 Page(s):230
AbstractPlus | Full Text: PDF(144 KB) IEEE CNF

3. **Reliability and design qualification of a sub-micron tungsten silicide E-Fuse**
Tonti, W.R.; Fifield, J.A.; Higgins, J.; Guthrie, W.H.; Berry, W.; Narayan, C.;
Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International
25-29 April 2004 Page(s):152 - 156
AbstractPlus | Full Text: PDF(456 KB) IEEE CNF

4. **Reliability of laser activated metal fuses in DRAMs**
Arndt, K.; Narayan, C.; Brintzinger, A.; Guthrie, W.; Lachtrupp, D.; Mauger, J.; Glimmer, D.; Lawn, S.; Dinkel, B.; Mitwalsky, A.;
Electronics Manufacturing Technology Symposium, 1999. Twenty-Fourth IEEE/CPMT
18-19 Oct. 1999 Page(s):389 - 394
AbstractPlus | Full Text: PDF(756 KB) IEEE CNF

5. **An on-chip self-repair calculation and fusing methodology**
Anand, D.; Cowan, B.; Farnsworth, O.; Jakobsen, P.; Oakland, S.; Ouellette, M.R.; Wheater, D.L.;
Design & Test of Computers, IEEE
Volume 20, Issue 5, Sept.-Oct. 2003 Page(s):67 - 75
AbstractPlus | References | Full Text: PDF(298 KB) IEEE JNL

6. **Product specific sub-micron E-fuse reliability and design qualification**
Tont, W.Ri.; Fifield, J.A.; Higgins, J.; Guthrie, W.H.; Berry, W.; Narayan, C.;
Integrated Reliability Workshop Final Report, 2003 IEEE International
20-23 Oct. 2003 Page(s):36 - 40
AbstractPlus | Full Text: PDF(447 KB) IEEE CNF

7. **Micro programmable built-in self repair for SRAMs**
Zappa, R.; Selva, C.; Rimondi, D.; Torelli, C.; Crestan, M.; Mastrodomenico, G.; Albani, L.;
Memory Technology, Design and Testing, 2004. Records of the 2004 International Workshop on
9-10 Aug. 2004 Page(s):72 - 77
AbstractPlus | Full Text: PDF(392 KB) IEEE CNF

Google API Proximity Search (GAPS)

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Find fuse within 3 word(s) of repair Search

in that order Sort by title Additional terms: verilog

Show All results, with up to 10 from each query Filter each query

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ArraytestMaker User Reference Manual [distance: 0]
repair, the â€œRepair **Verilog**â€□ model also must be generated. ... It is also possible to model memories for **fuse repair** in ArraytestMaker. This illustrated ...
http://www.genesystest.com/Artisan81.pdf - - Cached - Similar pages

ArraytestMaker User Reference Manual [distance: 0]
one where it is possible to choose between dynamic and **fuse repair** after the ... Simulators from Cadence and Synopsys like VCS, **Verilog**-XL and NCVerilog are ...
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http://www.genesystest.com/dolphin11.pdf - - Cached - Similar pages

Comit Systems - Fiesta CMBT [distance: 3]
Pass/Fail, Serial shift of **Fuse map for laser repair** ... **Verilog®** / VHDL RTL and Test Bench generation; Compatible with industry standard tools ...
http://www.comit.com/products/cmbt.htm - 23k - Cached - Similar pages

DeepChip Homepage [distance: 2]
The **Verilog** netlist written is also broken and cannot be legally read > back in to ... "It can do off-chip test > with laser **fuse-box repair** at manufacture. ...
http://www.deepchip.com/posts/0360.html - 59k - Cached - Similar pages

EEDesign.com - <B>Commentary:</B> Memory redundancy requires ... [distance: 0]
... At the program level, **fuse repair** may also require a wafer-cost adder associated ... Entry & Verification Solution Active-HDL 6.3 supports mixed VHDL,**Verilog**, C/C++ ...
http://www.eedesign.com/silicon/showArticle.jhtml?articleId=17408099&kc=6325 - 58k - Cached - Similar pages

Fiesta CMBT from Comit Memory BIST Controller [distance: 3]
Pass/Fail, Serial shift of **Fuse map for laser repair**. Debug and Engineering for characterization ... **Verilog®** / VHDL RTL and Test Bench generation ...
http://www.comit.com/products/brochures/FiestaCMBT.pdf - - Cached - Similar pages

Genesys Testware, Inc. [distance: 1]
Laser and electrical **fuse based repair** increases the complexity of physical design ... The compiler outputs consist of behavioral models in **Verilog** or VHDL, ...
http://www.genesystest.com/Pressrelease.html - 6k - Cached - Similar pages

MICROS SEMINAR [distance: 0]
Although the wafer-level laser-**fuse repair** method is the most widely used up ... In addition, we show how to reuse the given **Verilog** monitor module for the ...
http://micros.kaist.ac.kr/edu_activity/seminar/seminar.htm - 248k - Cached - Similar pages

Poster Session [distance: 0]

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((repair <and> fuse <and> verilog)<in>metadata)

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Results for "((verilog <and> simulation <and> path <and> fuse)<in>metadata)"

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((verilog <and> simulation <and> path <and> fuse)<in>metadata)

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((verilog <and> simulation <and> path)<in>metadata)

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» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **An architecture for a verilog hardware accelerator**
Burns, C.;
Verilog HDL Conference, 1996. Proceedings., 1996 IEEE International
26-28 Feb. 1996 Page(s):2 - 11
AbstractPlus | Full Text: PDF(704 KB) IEEE CNF

2. **Logic simulation methods for longest path delay estimation**
Maksimovic, D.M.; Litovski, V.B.;
Computers and Digital Techniques, IEE Proceedings-
Volume 149, Issue 2, March 2002 Page(s):53 - 59
AbstractPlus | Full Text: PDF(767 KB) IEE JNL

3. **A top down design environment for data-path design [FIR filter]**
Yamazaki, T.; Kondo, Y.;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International
27 Sept.-1 Oct. 1993 Page(s):266 - 269
AbstractPlus | Full Text: PDF(280 KB) IEEE CNF

4. **Property-specific testbench generation for guided simulation**
Gupta, A.; Casavant, A.E.; Ashar, P.; Liu, X.G.; Mukaiyama, A.; Wakabayashi, K.;
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific and the 15th International Conference on VLSI Design. Proceedings.
7-11 Jan. 2002 Page(s):524 - 531
AbstractPlus | Full Text: PDF(338 KB) IEEE CNF

5. **A Verilog simulation of the CDF DAQ system**
Schurecht, K.; Harris, R.; Sinervo, P.K.; Grindley, R.;
Nuclear Science Symposium and Medical Imaging Conference, 1991., Conference Record of the 1991 IEEE
2-9 Nov. 1991 Page(s):893 - 897 vol.2
AbstractPlus | Full Text: PDF(416 KB) IEEE CNF

6. **Fast cycle-accurate simulation and instruction set generation for constraint-based descriptions of programmable architectures**
Weber, S.J.; Moskewicz, M.W.; Gries, M.; Sauer, C.; Keutzer, K.;
Hardware/Software Codesign and System Synthesis, 2004. CODES + ISSS 2004. International Conference on
2004 Page(s):18 - 23
AbstractPlus | Full Text: PDF(545 KB) IEEE CNF

7. **Three alternative architectures of digital ratioed compressor design with application to inner-product processing**
Wang, C.-C.; Lee, P.-M.; Huang, C.-J.;

Computers and Digital Techniques, IEE Proceedings-
Volume 147, Issue 2, March 2000 Page(s):65 - 74

AbstractPlus | Full Text: PDF(548 KB) IEE JNL

8. **A comparison of two alternative architectures of digital ratioed compressor design for inner product processing**
Wang, C.-C.; Huang, C.J.; Lee, P.-M.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on
Volume 1, 30 May-2 June 1999 Page(s):161 - 164 vol.1

AbstractPlus | Full Text: PDF(252 KB) IEEE CNF

9. **Designing an asynchronous microcontroller using Pipefitter**
Blunno, I.; Lavagno, L.;
Computer Design: VLSI in Computers and Processors, 2002. Proceedings. 2002 IEEE International Conference on
16-18 Sept. 2002 Page(s):488 - 493

AbstractPlus | Full Text: PDF(573 KB) IEEE CNF

10. **High-level symbolic simulation using integer equations**
Gharehbaghi, A.M.; Hessabi, S.; Eshghi, M.R.;
Electrical and Computer Engineering, 2004. Canadian Conference on
Volume 3, 2-5 May 2004 Page(s):1241 - 1244 Vol.3

AbstractPlus | Full Text: PDF(436 KB) IEEE CNF

11. **A new design for high speed and high-density carry select adders**
Hashemian, R.;
Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on
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